

The rejection of Claims 1 and 33 is respectfully traversed in light of the following remarks.

Claims 1 and 33 are directed to a device and method, respectively, for channel coding in a communication system. Specifically, the channel coding device and method as recited in Claims 1 and 33 insert known bits in an input data bit stream, channel code the bit-inserted data bit stream, match the rate of the channel coded symbols to a given channel symbol rate, and then interleave the rate matched channel symbols in a manner that minimizes performance degradation caused by symbol repetition.

McCallister et al. teach a pilot bit generator (54) that produces an augmented secondary stream (col. 5 lines 18-20), and a puncture controller (58) that provides an output that couples to the pilot bit generator and informs pilot bit generator (54) when to insert pilot bit (56) (col 5 lines 29-31). Further, *McCallister et al.* disclose puncture controller (58) configured so that erasures do not include a pilot bit (col. 6 lines 25-26), and MUX (62) produces a secondary encoded stream (68) which includes non-systematic and systematic symbols generated from the zero-th information bit of each pent-tuple (48) (col. 6 lines 46-49). Furthermore, due to pilot bit insertion and puncturing, MUX (62) generates two symbols for each pent-tuple (48). Also, MUX (62) is configured so that only one of the two symbols it produces for each pent-tuple (48) is mapped per unit interval (col. 7 lines 8-12).

Regarding independent Claims 1 and 33, the Office Action asserts that *McCallister et al.* disclose a "bit inserter" (54) for inserting known pilot bits at predetermined positions, a "channel coder" (60) for generating convolutional code symbols, a "rate matcher" (58) for matching the coded symbol rate to a given channel symbol rate, and a "channel interleaver" (62) for interleaving the rate matched channel symbols. It is respectfully submitted that the "rate matcher" (58), which was described in the Office Action for matching the coded symbol rate to a given channel rate, is, in fact, a puncture controller (58) that "informs the pilot bit generator (54) when to insert a pilot bit" (Col. 5, Lines 29-31). In the present invention, specifically in Claims 1 and 33, the rate matcher is provided "for matching a rate of the coded

symbols to a given channel symbol rate". A channel interleaver is provided to interleave the rate matched symbols.

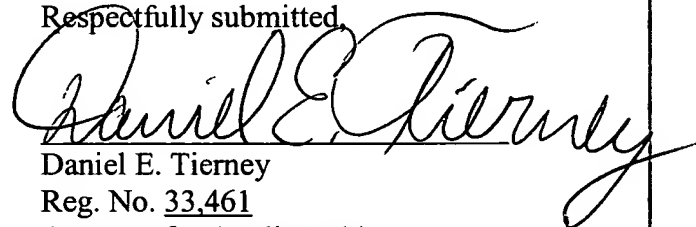
Moreover, in the claimed invention, "a bit inserter" inserts known bits in an input data bit stream at predetermined positions in order to transmit the coded source data at a specific data rate. In contrast, "the pilot bit generator" of *McCallister et al.* inserts bit-interleaved data. Further, the claimed bit inserter inserts bits in the coded source data to improve coder performance, and the bit-inserted data bit stream can be influential on the puncturing and repetition patterns. Moreover, *McCallister et al.* fail to disclose a channel interleaver that interleaves the rate matched channel symbols, and the MUX (62) of *McCallister et al.* cannot be equated to the claimed channel interleaver. Therefore, for at least these reasons, *McCallister et al.* do not anticipate Claims 1 and 33.

In view of the preceding remarks, it is respectfully submitted that Claims 1 and 33 are in condition for allowance. At least because of their dependence on Claims 1 and 33 respectively, dependent Claims 2-12, and 34-36 are also believed to be in condition for allowance.

CONCLUSION

Allowance of all pending claims is respectfully requested and prompt action on the merits is earnestly solicited. Should the Examiner feel that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner is urged to contact Applicants' attorney at the number given below.

Respectfully submitted,



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